

What is claimed is:

1. A method for manufacturing a transistor on a semiconductor substrate, said method comprising the steps of:

forming a dielectric layer on said semiconductor substrate;

etching said dielectric layer to form an opening in said first dielectric layer;

forming a gate oxide layer on said semiconductor substrate in said opening;

forming a barrier conductor along the surface of said opening;

forming a metal layer on said barrier conductor and refilled into said opening;

removing a portion of said metal layer and said barrier conductor to form a gate for said transistor;

removing said dielectric layer;

stripping said barrier conductor on sidewall of said gate;

forming lightly doped drain region in said semiconductor substrate;

forming sidewall spacer on sidewall of said gate; and

forming source and drain in said semiconductor substrate by ion implantation using said gate and spacer as masking.

2. The method of Claim 1, wherein said dielectric layer comprises silicon oxide, silicon oxynitride or silicon nitride.

3. The method of Claim 1, wherein said barrier conductor comprises titanium nitride, tungsten, aluminum or copper.

4. The method of Claim 1, wherein said metal layer comprises titanium.

5. A method for manufacturing a transistor on a semiconductor substrate, said method comprising the steps of:

forming a dielectric layer on said semiconductor substrate;

etching said dielectric layer to form an opening in said first dielectric layer;

forming a gate oxide layer on said semiconductor substrate in said opening;

forming a barrier conductor along the surface of said opening;

forming a metal layer on said barrier conductor and refilled into said opening;

removing a portion of said metal layer and said barrier conductor to form a gate for said transistor;

removing said dielectric layer;

forming lightly doped drain region in said semiconductor substrate by tilted angle ion implantation;

forming sidewall spacer on sidewall of said gate; and

forming source and drain in said semiconductor substrate by ion implantation using said gate and spacer as masking.

6. The method of Claim 5, wherein said dielectric layer comprises silicon oxide, silicon oxynitride, silicon nitride.

7. The method of Claim 5, wherein said barrier conductor comprises titanium nitride, tungsten, aluminum or copper.

8. The method of Claim 5, wherein said metal layer comprises titanium.

9. The method of Claim 5, wherein said titled angle ion implantation comprises LATIPS (large tilt-angle implanted punch-through stopper) technique.

10. A method for manufacturing a transistor on a semiconductor substrate, said method comprising the steps of:
forming a dielectric layer on said semiconductor substrate;

etching said dielectric layer to form an opening in said first dielectric layer;

forming a gate oxide layer on said semiconductor substrate in said opening;

forming a barrier conductor along the surface of said opening;

forming a metal layer on said barrier conductor and refilled into said opening;

removing a portion of said metal layer and said barrier conductor to form a gate for said transistor;

removing said dielectric layer;

stripping said stripping said barrier conductor on sidewall of said gate and forming under cut under said gate;

forming sidewall spacer on sidewall of said gate; and

forming lightly doped drain region in said semiconductor substrate by titled angle ion implantation; and

forming source and drain in said semiconductor substrate by ion implantation using said gate and spacer as masking.

11. The method of Claim 10, wherein said dielectric layer comprises silicon oxide, silicon oxynitride, silicon nitride.

12. The method of Claim 10, wherein said barrier conductor comprises titanium nitride, tungsten, aluminum or copper.

13. The method of Claim 10, wherein said metal layer comprises titanium.

14. The method of Claim 10, wherein said tilted angle ion implantation comprises LATIPS (large tilt-angle implanted punch-through stopper) technique.

~~15. A transistor on a semiconductor substrate, said method comprising the steps of:~~

~~a gate oxide formed on said semiconductor substrate;
a gate formed on said gate oxide, an under cut structure being formed under said gate, wherein said gate is consisted of a barrier conductor and a main gate structure;~~

~~spacer formed on sidewall of said gate and refilled into said under cut structure;~~

~~lightly doped region formed in said semiconductor substrate, and adjacent to said gate; and~~

~~source and drain formed in said semiconductor substrate, and adjacent to said lightly doped region.~~

~~16. The transistor of Claim 15, wherein said barrier conductor comprises titanium nitride, tungsten, aluminum or copper.~~

~~17. The transistor of Claim 15, wherein said main gate structure comprises titanium.~~

~~18. A transistor on a semiconductor substrate, said method comprising the steps of:~~

~~a gate oxide formed on said semiconductor substrate;
a gate formed on said gate oxide, wherein said gate is consisted of a barrier conductor and a main gate structure;
conductor spacer formed on sidewall of said gate;~~

~~dielectric spacer formed on sidewall of said conductor spacer;~~

~~lightly doped region formed in said semiconductor substrate, and adjacent to said gate; and~~

~~source and drain formed in said semiconductor substrate, and adjacent to said lightly doped region.~~

~~19. The transistor of Claim 18, wherein said barrier conductor comprises titanium nitride, tungsten, aluminum or copper.~~

~~20. The transistor of Claim 18, wherein said main gate structure comprises titanium.~~

~~21. The transistor of Claim 18, wherein said conductor comprises spacer comprises titanium nitride, tungsten, aluminum or copper.~~